Power and Linearity Performance of a Cascode InGaP/GaAs HBT Distributed Amplifier for Instrument Applications

Luciano Boglione

IEEE member – l.boglione@ieee.org

***Abstract* — This paper will describe the performance of a cascode InGaP/GaAs HBT distributed amplifier for instrument applications. In particular, the linearity of the distributed amplifier is considered. The compression point, the second and third harmonics, and the third order intercept point have been measured over different bias conditions. At nominal bias, the amplifier delivers a P1dB of 20dBm and a TOI of 30dBm up to 20GHz. This amplifier can achieve simultaneously some of the best results published in the literature.**

I. Introduction

Over the years, an impressive number of distributed amplifier designs have been published. The underlying theme is that the distributed amplifier can achieve very broadband performance by including the input and output capacitances of the active device into external transmission lines. The input and output transmission lines provide the required phase shift between consecutive devices. This phase shift is chosen such that constructive interference takes place and power is delivered from the source to the load [1].

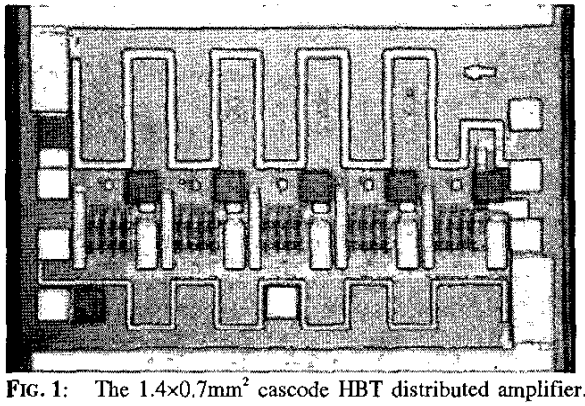

FIG. 1: The 1.4×0.7mm² cascode HBT distributed amplifier. On-chip capacitors can be seen above and below.

The main characteristic of the distributed amplifier is to have a very large bandwidth. Although the distributed amplifier is not the only topology that can achieve broadband performance [2],[3],[4], it is the most popular. Circuit solutions have been proposed to extend the bandwidth towards DC [5]; the upper limit is mostly determined by the device parasitics and consequently by the cut-off frequency of the transmission lines. Many works have focused on the noise performance, but fewer have investigated the trade offs related to the power and linearity performance of the distributed amplifier [6],[7],[8].

The goal of this paper is to provide data on the power and linearity performance of an HBT distributed amplifier. The particular amplifier developed in this work makes use of InGaP/GaAs HBTs and of the cascode configuration for each of its cells. Highlights of the design trade offs will be described, followed by the experimental results.

II. Circuit Fabrication & Design

The distributed amplifier (Fig.1) makes use of InGaP/GaAs HBTs fabricated by the Agilent Microwave Technology Center in Santa Rosa [9]. The devices are capable of ft on the order of 65GHz, fmax of 75GHz, and a breakdown voltage of about 8.5V. The minimum emitter size is 2μm×2μm. The process provides thin film resistors of 22Ω/□ and 250Ω/□, silicon nitride MIM capacitors of 0.39fF per μm² and backside vias.

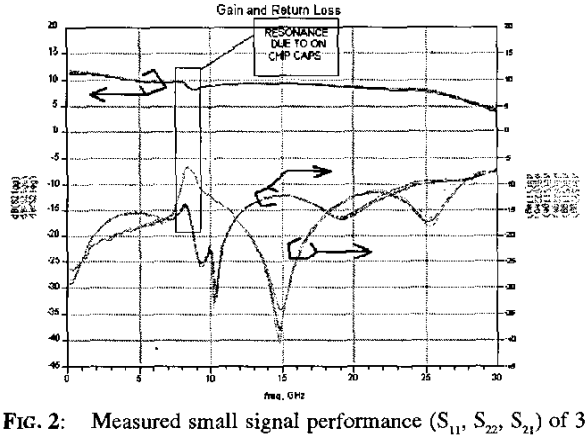

FIG. 2: Measured small signal performance (S_{11}, S_{22}, S_{21}) of 3 samples.

This amplifier's specs are suited for instrument applications: medium output power (P1dB=20dBm),

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large bandwidth (>20GHz) and high OIP3 over the entire bandwidth are the main goals of the design. No noise figure specification was required. Active loads on chip [5] have been considered to extend the bandwidth towards DC. This option has not been pursued because: 1) at the output, it would require higher bias voltage, with added power dissipation; 2) early estimates of their effect on linearity did not seem to be positive. Consequently, a standard design with passive loads has been adopted.

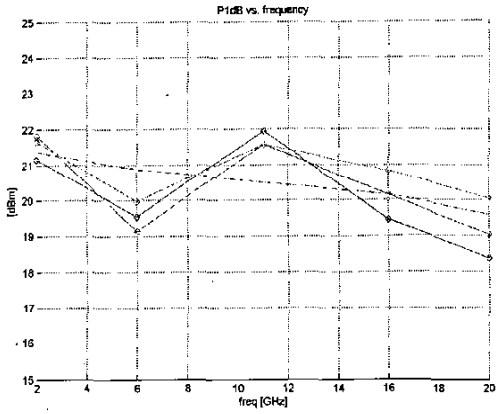

FIG. 3: Measured (solid + diamonds) vs. simulated (dashed) P1dB of 3 samples.

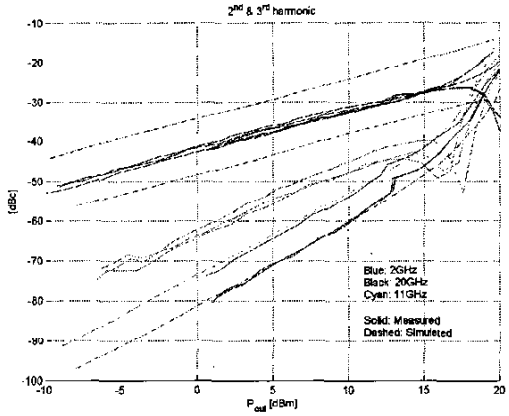

FIG. 4: Measured (3 samples) and simulated 2nd and 3rd harmonics referred to the output power of the fundamental.

The distributed amplifier is comprised of 5 cells, each with eight 16μm² HBTs. The total collector current is Icc=155mA (simulated) at Vcc=7V. A cascode topology for each cell is used in order to reduce the Miller effect of the common emitter transistor. The common base HBT is RF grounded by a capacitor. An external voltage Vadj controls the DC value of its base terminal through a 1:3 voltage divider. Its value also determines the partitioning of Vcc across the collector emitter terminals of the two HBTs. A large feedback resistance is used between collector and base of the common base transistor to improve stability. Its contribution to the determination of the base voltage is negligible.

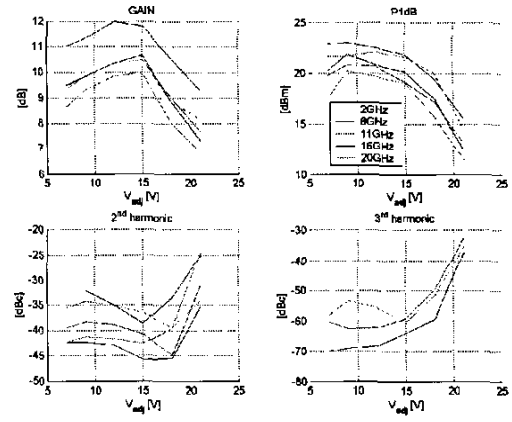

FIG.5: Variations of P1dB and harmonics with Vadj at Pout=10dBm.

In order to reduce the input capacitance, an RC network is inserted between the base and the input transmission line. This network provides a zero to cancel out the pole produced by the input resistance and capacitance of the common emitter transistor and allows the base to be biased through the input transmission line. The high gain available from the transistor is traded off for wider bandwidth. A small emitter resistor in each cell provides some series feedback. Although this resistor may improve linearity, it also introduces losses that may affect the power performance negatively.

Finally, the DC currents are delivered through the input and output ports by wafer probes coupled with bias tees. On chip capacitors have also been included to extend the lower limit of the bandwidth at the expense of the die size.

Simulations have been carried out with Agilent ADS ver. 190. The simulation predicts a small resonance that is caused by the on-chip capacitors [5]. The resonance does not affect the overall unconditional stability of the circuit.

Thermal behavior has been assessed at the time of the design and it has been found acceptable. Performance over temperature has not been investigated at this time.

III. RESULTS

The equipment used for testing the amplifier is composed of a HP8510 network analyzer, HP8565 power sources, HP8565 spectrum analyzer and ground-signal-ground 50GHz Picoprobes by GGB Industries. We tested the circuit with a fundamental frequency up to 20GHz.

A. Small signal performance

S_{21} is about 10dB and the –3dB frequency is 26GHz (Fig. 2). Input and output return loss is better than 10dB. Isolation is better than 25dB. Good repeatability has been observed over a small sample of circuits from 2 different wafers.

B: Output power & harmonics

Fig. 3 and 4 show the measured power and harmonic results vs. simulation: P1dB compression point is around 20dBm as expected; the 2nd harmonic is better than -30dBc; and the 3rd harmonic is better than -40dBc up to Pout=10dBm.

The power performance of the distributed amplifier has also been measured over different values of Vadj. Fig. 5 shows the results at a nominal current Icc=158mA and collector voltage Vcc=7V, and demonstrates that the 2nd and 3rd harmonics (referred to Pout) have a minimum at the nominal Vadj=15V.

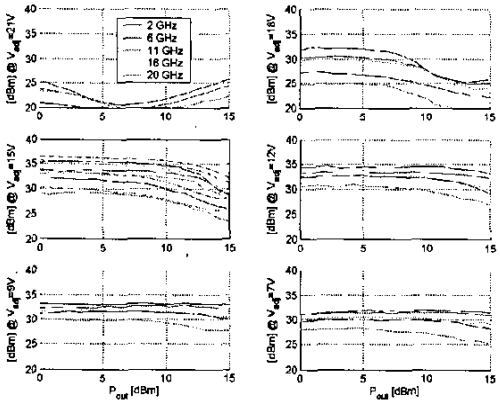

FIG. 6: Output TOI vs. Pout over output Vadj and frequency. The plot at nominal Vadj=15V shows the simulation results (dashed).

C. Third Order Output Intercept Point

The same system outlined above is used with two power sources and a different calibration to measure the third order intercept point at the output (OIP3). Results over different values of Vadj are presented at constant nominal Icc (≈158mA) and Vcc (7V).

Fig. 6 shows the measured data vs. Vadj: OIP3 is little less than 30dBm (output) over the measurable bandwidth of 20GHz at Pout = 10dBm and Vadj=15V. Lowering Vadj improves OIP3 and reduces its frequency dependence.

Fig. 7 shows OIP3 vs. frequency or Vadj at constant Pout (10dBm). Results are slightly better when Pout levels are less than 10dBm (Fig. 6). An optimal range of Vadj between 9V and 12V exists to increase OIP3 above 30dBm for frequencies up to 20GHz. The trade off is with gain, P1dB and the 2nd and 3rd harmonics (see Fig. 5).

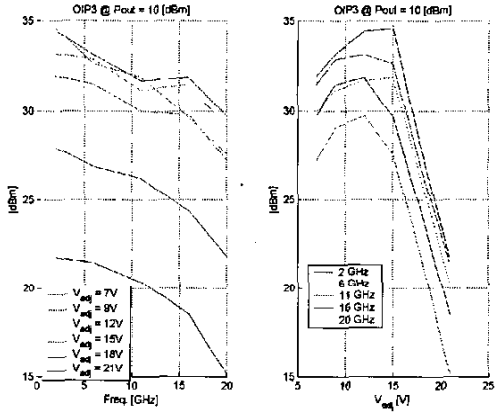

FIG. 7: OIP3 performance at constant Pout.

IV. DISCUSSION

In order to compare the performance of this distributed amplifier with other state of the art circuits, it is important to remember that this amplifier must meet the conflicting requirements that are typical of instrument applications, such as bandwidth, power, gain, linearity, etc. In order to understand its contribution, several metrics should be considered simultaneously.

Table I collects published results along with metrics found in the literature that help to evaluate the performance of our amplifier in comparison to similar circuits. We have also defined new metrics to try to capture the circuit's bandwidth response. The new metrics are defined by multiplying the old one by the circuit bandwidth — a value easily available in the literature.

The table has been populated with similar circuits in terms of band, power and/or linearity. We have not

limited ourselves to either the same technology or the same topology. P1dB and bandwidth are similar across the selected references.

Notice that the first work referenced in the table was published in 1992 [8]. Its OIP3 is still state of the art! We offer a couple of reasons to explain a 10 years long gap: 1) linearity results over large bandwidths are rarely reported in the literature; 2) over the years, distributed amplifiers' typical applications have shifted from analog to digital [10], where linearity is not a "money-spec".

A color code has been used in Table I to identify the best performances. This work scores two *1st*, one *2nd* and one *3rd best* out of 6 metrics over DC to 20GHz. The table demonstrates that our distributed amplifier excels at several metrics that "specialized" amplifiers such as [7], [8] optimize at the expense of other metrics.

V. Conclusion

The performance of a highly linear amplifier has been demonstrated. High output intercept point over a wide bandwidth is achieved at a constant P1dB of 20dBm. An evaluation with other amplifiers has been carried out to show state of the art performance of this amplifier for several metrics.

Acknowledgement

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Table 1: Color code is: Red=1st best; Blue=2nd best; Green=3rd best. OIP3 values in ref. [7] and [8] are average values.

Ref.	Year	S11	S22	S21	P1dB	OIP3	fmin	fmax	Pdc	Size	BW	METRICS: Gain/size	BW*Gain /size	OIP3 /PDC	BW*OIP3 /PDC	P1dB /PDC	BW*P1dB/ PDC	Technology
		dB	dB	dB	dBm	dBm	GHz	GHz	mW	mm2	GHz	dB/mm2	GHz*dB/ mm2	[-]	GHz	[-]	GHz	
THIS WORK	2002	-10	-10	10	20	30	0.05	26.5	1085	0.98	26.5	10.20	269.98	0.92	24.38	0.09	2.44	GaAs HBT
[8]	1992	-12	-12	6	18.5	37.5	6	16	570	3.3	10	1.82	18.18	3.87	98.66	0.12	1.24	GaAs MESFET
		-7	-7	8	20.5	20.5	6	12	692	1.95	6	4.10	24.62	0.16	0.97	0.16	0.97	GaAs MESFET
[11]	1990	-9.5	-10	11.7	17	22	6	18	560	7.2	12	1.63	19.50	0.28	3.40	0.09	1.07	GaAs FET
[12]	1990	-10	-8	4	10	-	9	70	-	0.5	61	8.00	488.00	-	-	-	-	pHEMT
[7]	1990	-10	-10	7.5	13	33	5	11	158	7.69	6	0.98	5.85	12.63	75.77	0.13	0.76	GaAs HBT
		-10	-10	10	7.5	20	0.05	9	50	4.5	8.95	2.22	19.89	2.00	17.90	0.11	1.01	GaAs HBT
[6]	1988	-10	-10	4	20	-	14	37	-	2.94	23	1.36	31.29	-	-	-	-	GaAs FET